

# Low Power 3D Magnetic Sensor with I<sup>2</sup>C Interface

## TLV493D-A1B6 3D Magnetic Sensor

### 3D Magnetic Sensor

#### Data Sheet

Rev. 1.1, 2019-04-09

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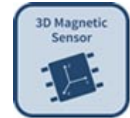
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Product Description

# 1 Product Description



## 1.1 Target Applications

The 3D magnetic sensor TLV493D-A1B6 offers accurate three-dimensional sensing with extremely low power consumption in a small 6-pin package. With its magnetic field detection in x, y, and z-direction the sensor reliably measures three-dimensional, linear and rotation movements. Applications include joysticks, control elements (white goods, multifunction knobs), or electric meters (anti tampering) and any other application that requires accurate angular measurements or low power consumptions.

The integrated temperature sensor can furthermore be used for plausibility checks.

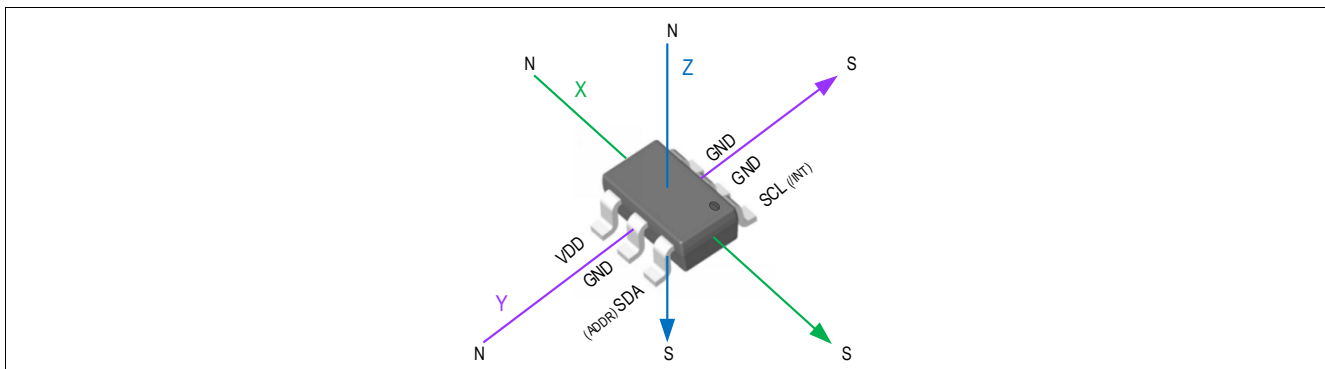


Figure 1 All three Sensitive Directions Bx, By and Bz

## 1.2 Features

- 3D magnetic sensing
- Very low power consumption = 10  $\mu$ A during operations (10 Hz, typ.)
- Power down mode with 7 nA power consumption
- Digital output via 2-wire based standard I<sup>2</sup>C interface up to 1 MBit/sec
- 12-bit data resolution for each measurement direction
- Bx, By and Bz linear field measurement up to  $\pm$ 130 mT
- Excellent matching of X/Y measurement for accurate angle sensing
- Variable update frequencies and power modes (configurable during operation)
- Supply voltage range = 2.8 V...3.5 V, Temperature range  $T_j = -40^{\circ}\text{C} \dots 125^{\circ}\text{C}$
- Small, industrial 6 pin TSOP package
- Triggering by external  $\mu$ C possible
- Interrupt signal available to wake up a microcontroller
- Temperature measurement

Table 1 Ordering Information

Product Name	Marking	Ordering Code	Package
3D Magnetic Sensor TLV493D-A1B6	VA (serie)	SP001286056	PG-TSOP-6-6-5

## 2 Functional Description

### 2.1 General

Description of the Block diagram and its functions.

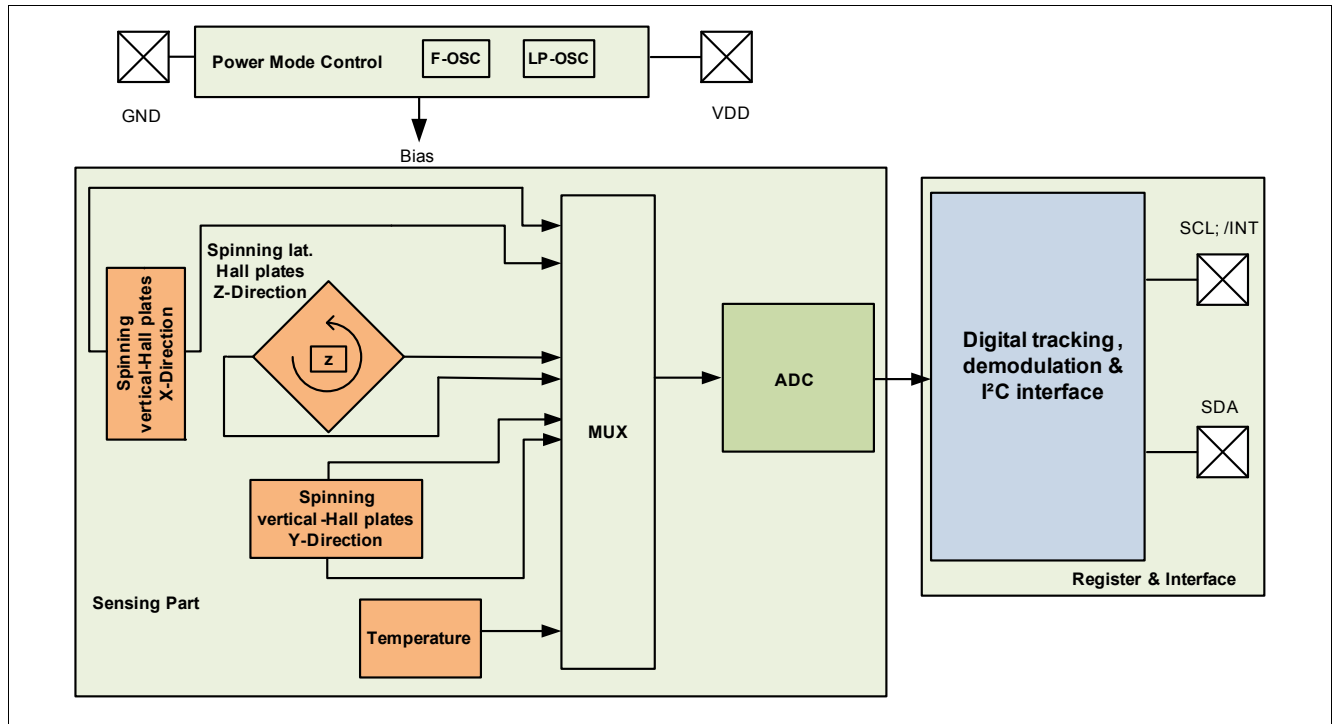


Figure 2 Block Diagram

The IC consists of three main function units containing the following building blocks:

- The power mode control system, containing a low-power oscillator, basic biasing, accurate reset, undervoltage detection and a fast oscillator.
- The sensing part, containing the HALL biasing, HALL probes with multiplexers and successive tracking ADC. Furthermore a temperature sensor is implemented.
- The I<sup>2</sup>C interface, containing the register file and I/O pads.

#### 2.1.1 Power Mode Control

The power mode control provides the power distribution in the IC, a power-on reset function and a specialized low-power oscillator clock source. Additionally it is handling the start-up behavior.

- On start-up this unit:
  - activates the biasing, provides an accurate reset detector and fast oscillator.
  - interprets the applied voltage level on ADDR pin as logical “0” or “1”. This determines one of two possible I<sup>2</sup>C bus addresses to access the sensor.
  - sensor enters power down mode (configured via I<sup>2</sup>C interface).

*Note: After supplying the sensor (= power up) the sensor enters the mode power down by default.*

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## Functional Description

- After re-configuration to one of the operating modes a measurement cycle is performed regularly containing of:
  - starts the internal biasing, checks for reset condition and provides the fast oscillator
  - provides the HALL biasing
  - the measurement of the three HALL probe channels sequentially incl. temperature (default = activated)
  - and enters the configured mode again

In any case functions are only executed if the supply voltage is high enough, otherwise the reset circuit will halt the state machine until the level is reached and restarts its operation afterwards. The functions are also restarted if a reset event occurs in between.

### 2.1.2 Sensing Part

Performs the measurements of the magnetic field in X, Y and Z direction. Each X, Y and Z-HALL probe is connected sequentially to a multiplexer, which is then connected to an Analog to Digital Converter (ADC). Optionally, the temperature is determined as well after the three HALL channels. The current consumption decreases by -25 % when temperature measurement is deactivated.

Functional Description

## 2.2 Pin Configuration (top view)

Figure 3 shows the pinout of the TLV493D-A1B6.

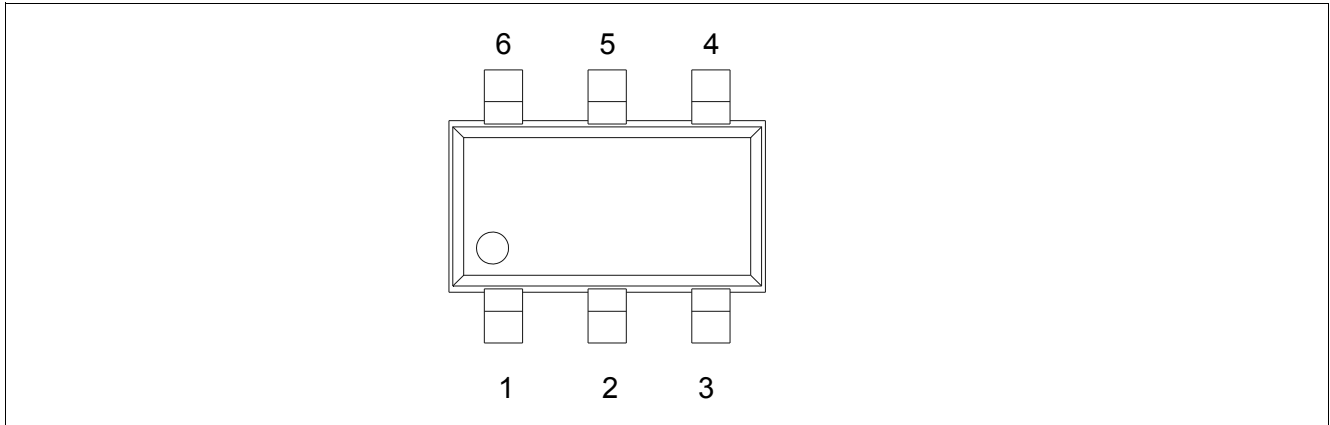


Figure 3 Pinout

Table 2 TSOP-6 Pin Description and Configuration (see Figure 1)

Pin No.	Name	Description
1	SCL /INT	Interface serial clock pin (input) Interrupt pin, signals a finished measurement cycle
2	GND	connect to GND
3	GND	Ground Pin
4	VDD	Supply Pin
5	GND	connect to GND
6	SDA ADDR	Interface serial data pin (input/output), open drain Sensor ID configuration during power up

## 2.3 Definition of Magnetic Field

A positive field is considered as South-Pole facing the corresponding Hall element.

Figure 4 shows the definition of the magnetic directions X, Y, Z of the TLV493D-A1B6.

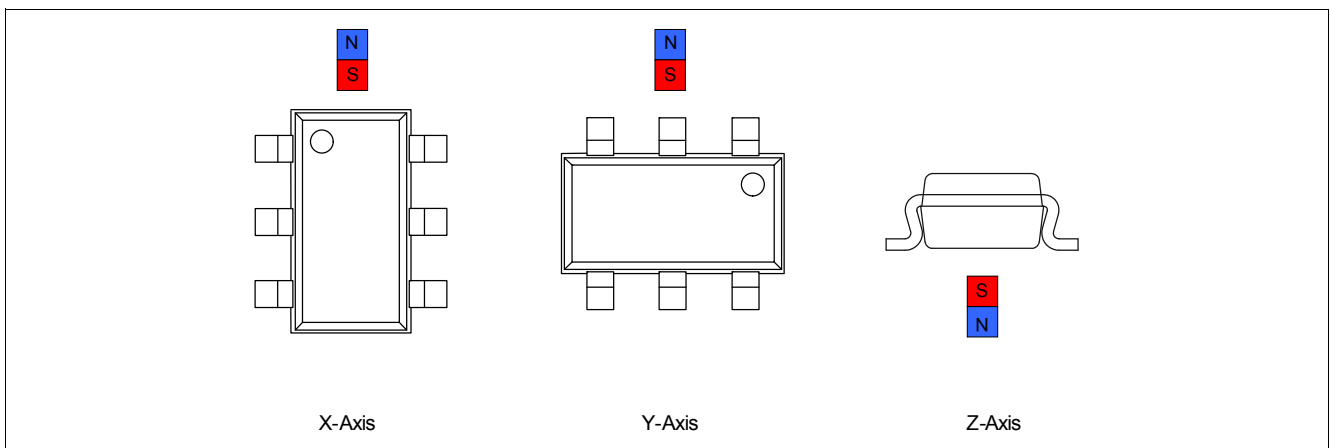


Figure 4 Definition of Magnetic Field Direction



## 2.4 Sensitive Area

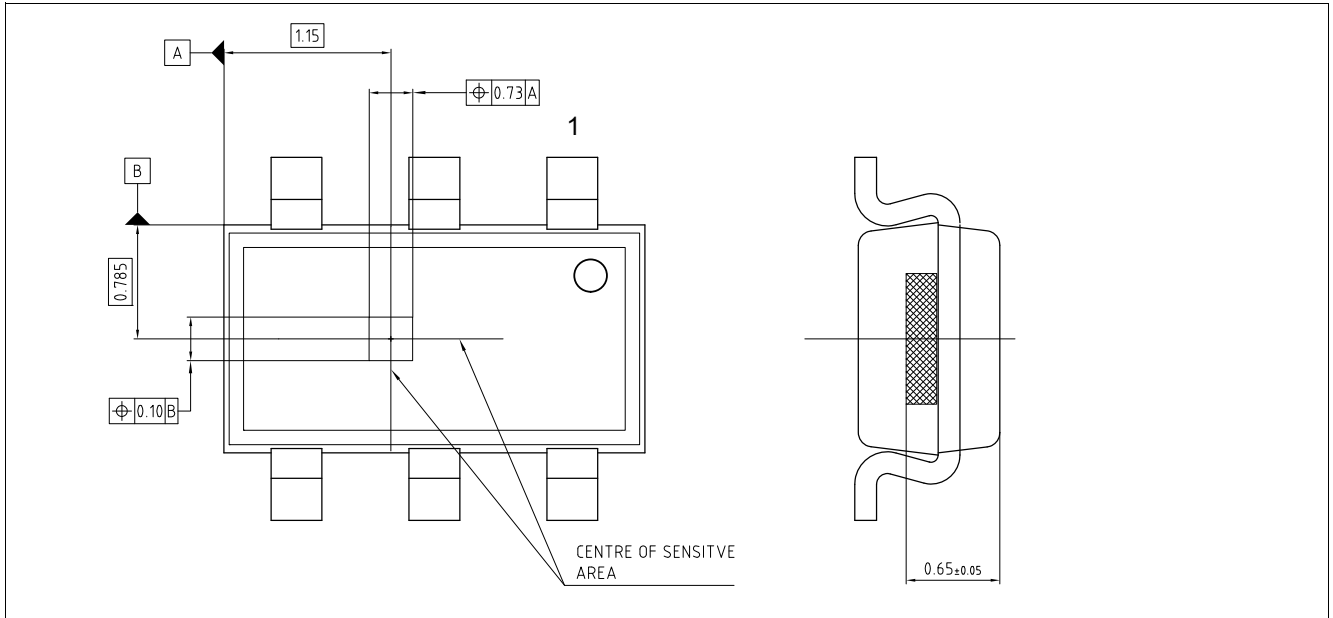


Figure 5 Center of Sensitive Area

Functional Description

## 2.5 Application Circuit

The use of an interrupt line is optional, but highly recommended to ensure proper and efficient readout of the sensor data.

The pull-up resistors  $R_1$  &  $R_2$  of the I<sup>2</sup>C bus have to be set in a way to keep the rise- and fall time specification of the interface bus parameters (see specification section) with the parasitic capacitive load of the actual setup.

The serial resistances  $R$  between SDA /SCL & Pull up  $R_1/R_2$  may be used to avoid reflections on longer bus lines causing ground bouncing on sensor side and communication issues.

The series resistance  $R$  between and the SCL  $\mu$ C pin and the pull up resistor  $R_2$  together with the capacitance  $C_2$  to ground may provide additional EMC filtering if required.

Please note: too small resistive values for  $R_{1/2}$  have to be prevented to avoid unnecessary power consumption during interface transmissions, especially for low-power applications. The additional capacitor  $C_2$  on the SCL line will limit the maximum possible bitrate on the bus.

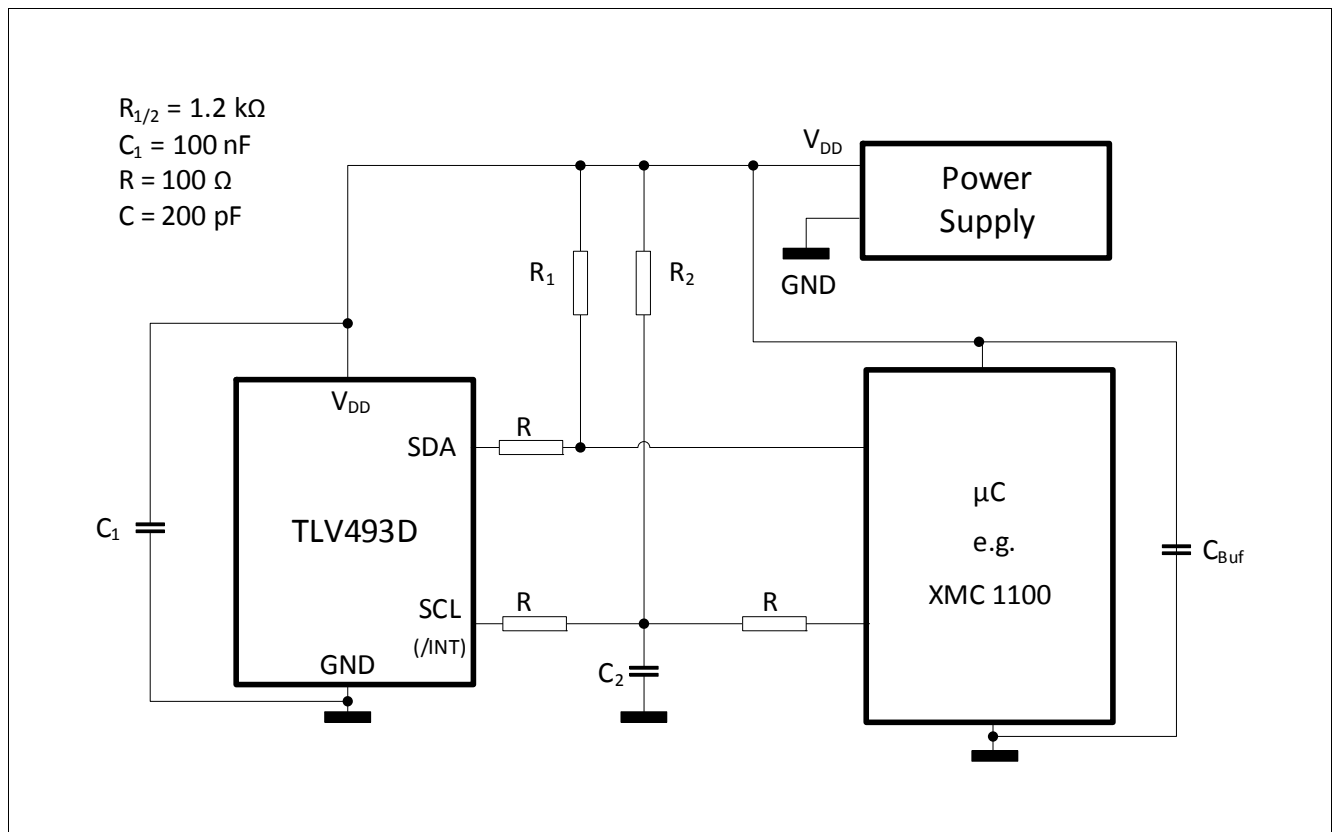


Figure 6 Application Circuit with external Power Supply and  $\mu$ C

For additional EMC precaution in harsh environments,  $C_1$  may be implemented by two 100 nF capacitors in parallel, which should be already given by  $C_{Buf}$  near the  $\mu$ C and/or power supply.

Specification

### 3 Specification

#### 3.1 Absolute Maximum Ratings

**Attention:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions the voltage on  $V_{DD}$  pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.

**Table 3 Absolute Maximum Ratings**

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Junction temperature	$T_j$	-40	–	125	°C	
Voltage on VDD	$V_{DD}$	-0.3	–	3.5	V	
Magnetic field	$B_{max}$	–	–	1	T	
Voltage range on any pin to GND	$V_{max}$	-0.1	–	3.5	V	open-drain outputs are not current limited

**Table 4 ESD Protection<sup>1)</sup> ( $T_a = 25^\circ\text{C}$ )**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM) <sup>2)</sup>	$V_{ESD}$	-1.5	–	1.5	kV	R = 1.5 k $\Omega$ , C = 100 pF
ESD voltage (CDM) <sup>3)</sup>		–	–	750	V	for corner pins
		–	–	500	V	all pins

- 1) Characterization of ESD is carried out on a sample basis, not subject to production test.
- 2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.
- 3) Charged Device Model (CDM), ESD susceptibility according to JEDEC JESD22-C101.

#### 3.2 Operating Range

**Table 5 Operating Range**

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Operating temperature	$T_j$	-40	–	125	°C	$T_j = T_a + 3^\circ\text{C}$ as worst case assumption
Supply voltage	$V_{DD}$	2.8	3.3	3.5	V	see Note below
Reset level	$V_{res}$	–	2.2	–	V	see Note below

Specification

To provide these ultra low power consumption figures, the chip does not use a classic (and current consuming) reset concept. The implemented reset focus is on ensuring a proper supply for the ADC operation only (so it inhibits the ADC reliably until the sensor supply is high enough). Thus, the sensor rely on a proper supply ramp including  $I_{DD-PUP}$  current consumption during power-on to ensure it is initialized correctly. The I<sup>2</sup>C reset feature of the sensor shall be used by the  $\mu$ C after power-up. If supply monitoring is used in the system (e.g. brown-out detector etc.) it is also recommended to use the I<sup>2</sup>C reset of the sensor upon events detected by this monitor.

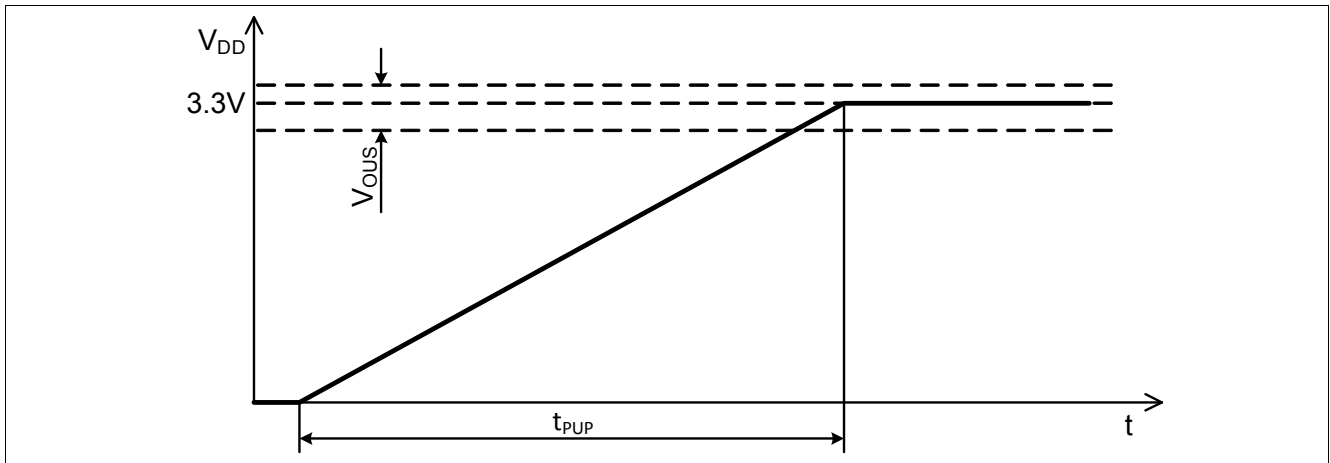


Figure 7  $V_{DD}$  power up and power-cycle for high availability

Table 6  $V_{DD}$  power up and power-cycle

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Power Up ramp time	$t_{PUP}$	-	-	10	$\mu$ s	
Power Up over-undershoot	$V_{OUS}$	3	3.3	3.5	V	Envelope which must not be exceeded at the end of a Power Up.
Power Up current consumption	$I_{DD-PUP}$	-	3.7	-	mA	Current consumption during $t_{PUP}$

Specification

### 3.3 Electrical Characteristics

Note: All specification parameters refer to 3.3 V  $\pm 5\%$  nominal supply  $V_{DD}$  on the pins directly. Typical values refer to 25°C and to 3.3 V  $\pm 5\%$  nominal supply.

**Table 7 Electrical Setup**

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Supply current <sup>1)</sup>	$I_{DD}$	-	7	100	nA	power down mode (default after power on), all off
		-	10	-	$\mu$ A	ultra low power mode
		-	80	-	$\mu$ A	low power mode
Average operating current	$I_{DD\_op}$	-	3.7	-	mA	peak during ADC measurements for about 270 $\mu$ s <sup>2) 3)</sup>
Input voltage low threshold	$V_{IL}$	-	-	20	% $V_{DD}$	all input pads
Input voltage high threshold	$V_{IH}$	70	-	-	% $V_{DD}$	all input pads
Input voltage hysteresis threshold	$V_{I\_Hyst}$	5	-	-	% $V_{DD}$	all input pads
Output voltage low level @ 3 mA load	$V_{OL}$	-	-	0.4	V	all output pads, static load
Fall time SDA/SCL signal <sup>4)</sup>	$t_{FALL}$	-	0.25 <sup>5)</sup>	0.3	$\mu$ s	0.3 $\mu$ s for 400 kHz mode (or may require less C load)
Rise time SDA/SCL signal <sup>4)</sup>	$t_{RISE}$	-	0.5 <sup>5)</sup>	-	$\mu$ s	R = 1.2 k $\Omega$
Output high level	$V_{OH}$	-	$V_{DD}$	-	V	given by ext. pull-up resistor

- 1) Average values
- 2) During power down mode the current consumption is about 7 nA
- 3) Current at Pull ups needs to be considered for power supply dimensioning, consider minimum 10 mA for the power supply for the sensor only
- 4) Dependent on used R-C-combination
- 5) For given AppCircuit; Capacitive load (parasitics and discrete caps used) for each bus line = 200 pF (SDA, SCL)

Note: The average supply current  $I_{DD}$  in the low power modes and I<sup>2</sup>C triggered mode will decrease by about 25% when the temperature measurement is disabled.

Specification

3.4 Temperature Measurement (default = activated)

Table 8 Temperature Measurement Characteristics

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Digital value @ 25°C <sup>1)</sup>	$T_{25}$	-	340	-	LSB	
Resolution 12 bit	$T_{Res12}$	-	1.1	-	°C/LSB	
Accuracy	$T_{ACC}$	-	±10	-	°C	

1) Theoretical possible measurement range from -50°C to 150°C

Interface and Timing Description

## 4 Interface and Timing Description

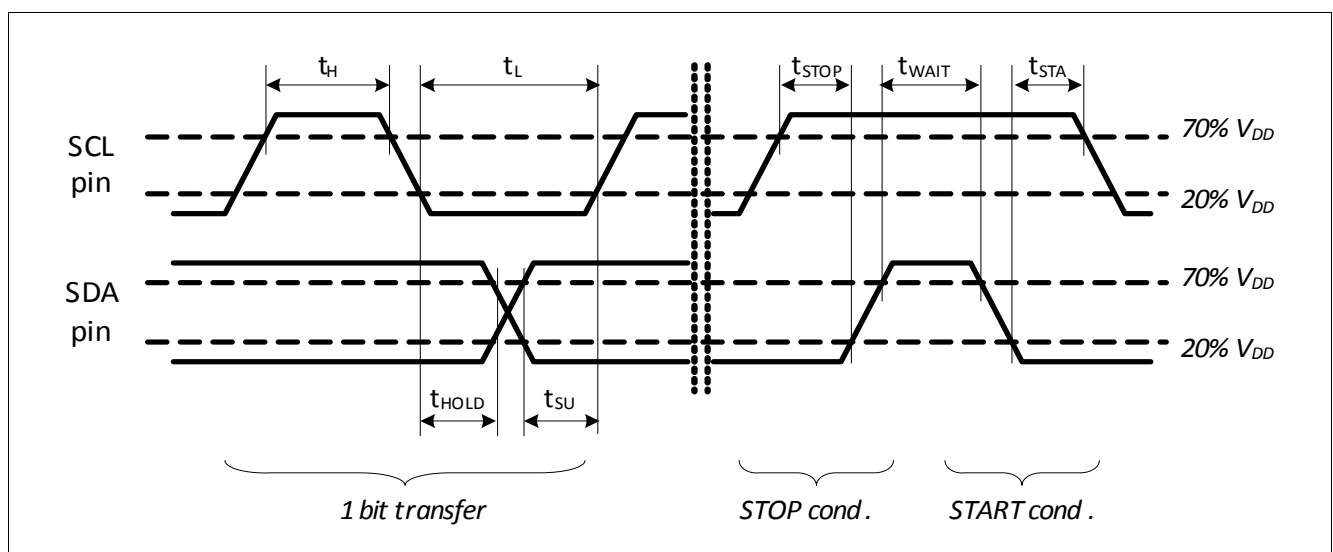
This chapter refers to how to set the boundary conditions in order to establish a proper interface communication.

**Table 9** Interface and Timing<sup>1)</sup>

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Update rate X, Y, Z	$f_{Ur}$	-	3.3	-	kHz	max. ADC conversion rate
Update rate (all axis), ultra low p.	$f_{Ur\_ulp}$	-	10	-	Hz	int. triggered
Update rate (all axis), low p.	$f_{Ur\_lp}$	-	100	-	Hz	int. triggered
End-of-Conversion /INT pulse	$t_{INT}$	-	1.5	-	$\mu$ s	low-active (when activated)
Internal clock accuracy	$t_{clk\_E}$	-25	-	25	%	all above timing parameters
Allowed I <sup>2</sup> C bit clock frequency <sup>2)</sup>	$f_{I2C\_clk}$	-	400	1000	kHz	400 kHz is I <sup>2</sup> C fast mode
Low period of SCL clock	$t_L$	0.5	-	-	$\mu$ s	1.3 $\mu$ s for 400 kHz mode
High period of SCL clock	$t_H$	0.4	-	-	$\mu$ s	0.6 $\mu$ s for 400 kHz mode
SDA fall to SCL fall hold time (hold time start condition to clock)	$t_{STA}$	0.4	-	-	$\mu$ s	0.6 $\mu$ s for 400 kHz mode
SCL rise to SDA rise su. time (setup time clock to stop condition)	$t_{STOP}$	0.4	-	-	$\mu$ s	0.6 $\mu$ s for 400 kHz mode
SDA rise to SDA fall hold time (wait time from stop to start cond.)	$t_{WAIT}$	0.4	-	-	$\mu$ s	0.6 $\mu$ s for 400 kHz mode
SDA setup before SCL rising	$t_{SU}$	0.1	-	-	$\mu$ s	
SDA hold after SCL falling	$t_{HOLD}$	0	-	-	$\mu$ s	

1) Not subject to production test - verified by design/characterization

2) Dependent on R-C-combination on SDA and SCL. Ensure reduced capacitive load for speeds above 400 kHz.



**Figure 8** I<sup>2</sup>C Timing Specification

Interface and Timing Description

**Managing correct sensor read outs by the  $\mu$ C:**

This sensor does not incorporate shadow-buffers for readout. Thus, it is mandatory to read the sensor data not during a running conversion to avoid corrupted reads. Ideally, the /INT feature is enabled together with the low-power or ultra-low power mode and the  $\mu$ C reads the data after the /INT pulse was asserted by the sensor. Furthermore, the readout needs to be finished before a new conversion is started and the /INT will be asserted again (if the readout is finished 1 ms before a new /INT pulse, this will be sufficient).

**Conversion register value to magnetic field and temperature value:**

The conversion is realized by the two's complement. Please use following table for transformation:

**Table 10 Conversion table for 12Bit**

	MSB	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	LSB
	-2048	1024	512	256	128	64	32	16	8	4	2	1
e.g.	1	1	1	1	0	0	0	0	1	1	1	1

Example for 12Bit read out: 1111 0000 1111:  $-2048 + 1024 + 512 + 256 + 0 + 0 + 0 + 0 + 8 + 4 + 2 + 1 = -241$  LSB

Calculation to mT:  $-241 \text{ LSB} * 0.098 \text{ mT/LSB} = -23.6 \text{ mT}$

For further information and a detailed I<sup>2</sup>C bitmap please refer to user manual.



Magnetic Characteristics

## 5 Magnetic Characteristics

**Table 11 Initial Magnetic Characteristics<sup>1)</sup>**

Values for 25°C, 0 h and  $V_{DD} = 3.3$  V

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Usable magnetic linear range <sup>2)</sup>	$B_{xyz\_LIN}$	–	±130	–	mT	Bx, By and Bz
Offset	$B_O$	-1	±0.2	1	mT	Bx, By and Bz
Sensitivity	$S_x, S_y, S_z$	–	10.2	–	LSB <sub>12</sub> / mT	Bx, By and Bz; (12bit)
Resolution 12-bit readout <sup>3)</sup>	Res <sub>12</sub>	–	98	–	μT/ LSB <sub>12</sub>	
Resolution 8-bit readout <sup>3)</sup>	Res <sub>8</sub>	–	1.56	–	mT/ LSB <sub>8</sub>	
Magnetic noise (rms)	$B_{ineff}$	–	0.1	–	mT	rms = 1 sigma
Magnetic hysteresis <sup>2)</sup>	$B_{HYS}$	–	1	–	LSB <sub>12</sub>	due to quantization effects

1) Magnetic test on wafer level. It is assumed that initial variations are stored and compensated in the external μC during module test and calibration.

2) Not subject to production test - verified by design/characterization.

3) Resolution is calculated as 1/Sensitivity (and multiplied by 16 for 8-bit value)

**Table 12 Sensor Drifts<sup>1)</sup>**

Values for  $V_{DD} = 3.3$  V ±5 %,  $T_j = -40$  to 125°C, static magnetic field within usable linear range

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Sensitivity drift	$S_{x_D}, S_{y_D}, S_{z_D}$	–	±20	–	%	Bx, By and Bz
Offset drift	$B_{O\_D}$	-1	±0.2	1	mT	Bx, By and Bz; @ 0mT
X to Y magnetic matching drift <sup>2)</sup>	$M_{XY\_D}$	–	±5	–	%	
X/Y to Z magnetic matching drift <sup>2)</sup>	$M_{X/YZ\_D}$	–	±20	–	%	
Temperature compensation <sup>3)</sup>	TC	–	0	–	ppm/K	Bx, By and Bz
DNL (Differential Non Linearity) <sup>1)</sup>	DNL	–	±5	–	LSB <sub>12</sub>	Bx, By and Bz
INL (Integral Non Linearity) <sup>1)</sup>	INL	–	0.1	–	%FSR <sup>4)</sup>	Bx, By and Bz

1) Not subject to production test, verified by design/characterization. Drifts are changes from the initial characteristics due to external influences.

2) See the magnetic matching definition in [Equation \(5.1\)](#) and [Equation \(5.2\)](#).

3) Can be changed by I<sup>2</sup>C command during operation; further typical values are -2000, -1000, 500 ppm/K

4) The FSR is calculated as ±2048 · Res<sub>12</sub>

Characteristical

Equation for parameter “X to Y magnetic matching”: (5.1)

$$M_{XY} = 100 \cdot 2 \cdot \frac{Sx - Sy}{Sx + Sy} [\%]$$

Equation for parameter “X/Y to Z magnetic matching”: (5.2)

$$M_{X/YZ} = 100 \cdot 2 \cdot \frac{Sx + Sy - 2 \cdot Sz}{Sx + Sy + 2 \cdot Sz} [\%]$$

## 6 Characteristical

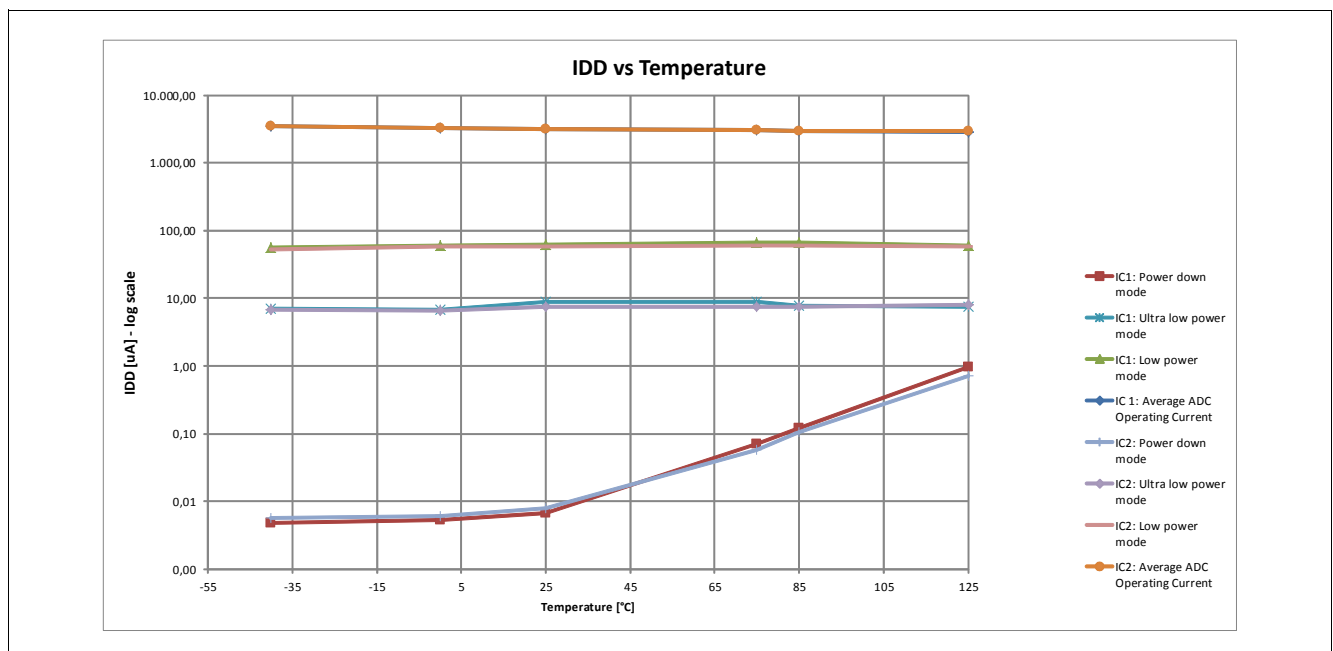


Figure 9  $I_{DD}$  versus Temperature

Package Information

## 7 Package Information

### 7.1 Package Parameters

Table 13 Package Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Thermal resistance Junction ambient	$R_{thJA}$	–	–	200	K/W	Junction to air <sup>1)</sup> for PG-TSOP6-6-5
Thermal resistance Junction lead	$R_{thJL}$	–	–	100	K/W	Junction to lead for PG-TSOP6-6-5
Soldering moisture level	MSL 1					260°C <sup>2)</sup>

1) according to Jecdec JESD51-7

2) suitable for reflow soldering with soldering profiles according to JEDEC J-STD-020D.1 (March 2008)

### 7.2 Package Outlines

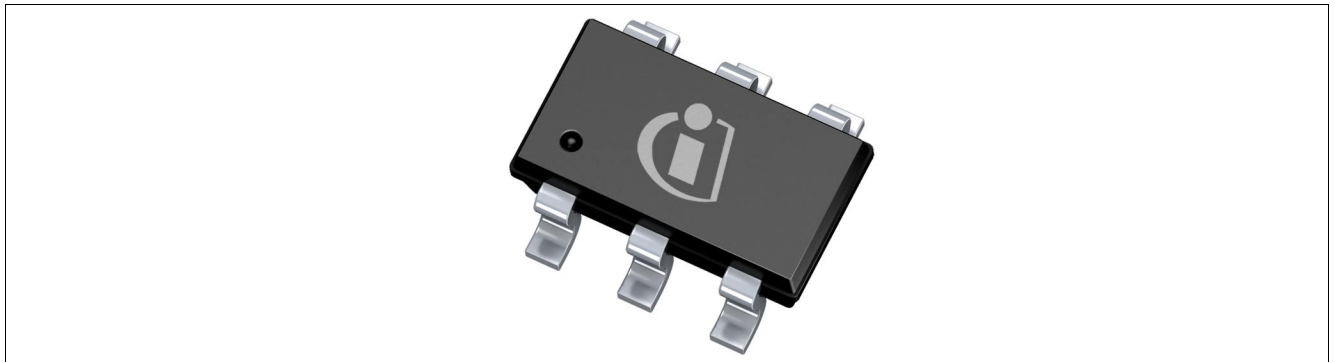


Figure 10 Image of TLV493D-A1B6 in PG-TSOP-6-6-5

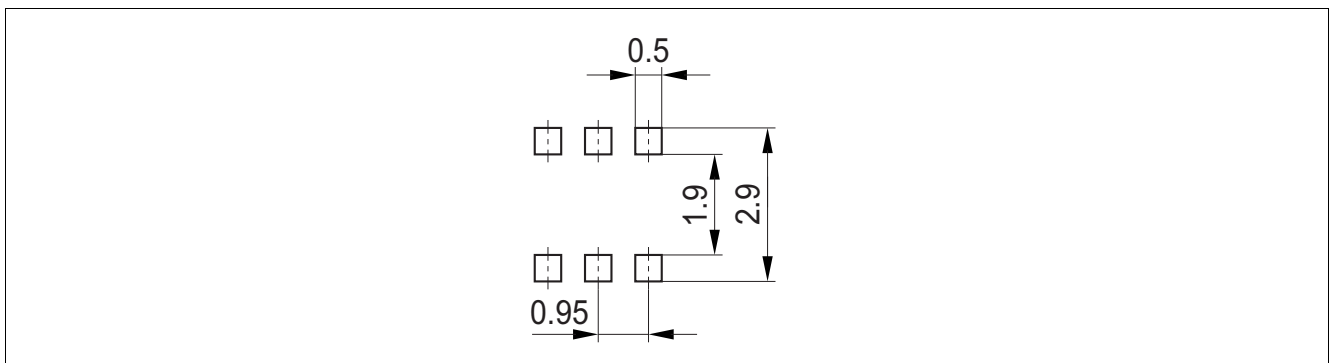


Figure 11 Footprint PG-TSOP-6-6-5, Reflow Soldering (all dimensions in mm)

Package Information

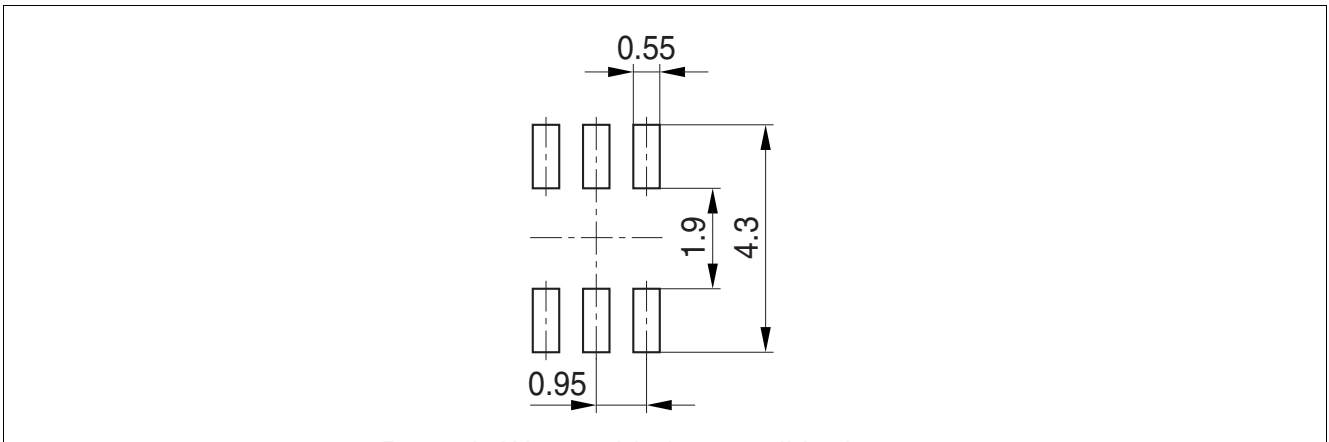


Figure 12 Footprint PG-TSOP-6-6-5, Wave Soldering (all dimensions in mm)

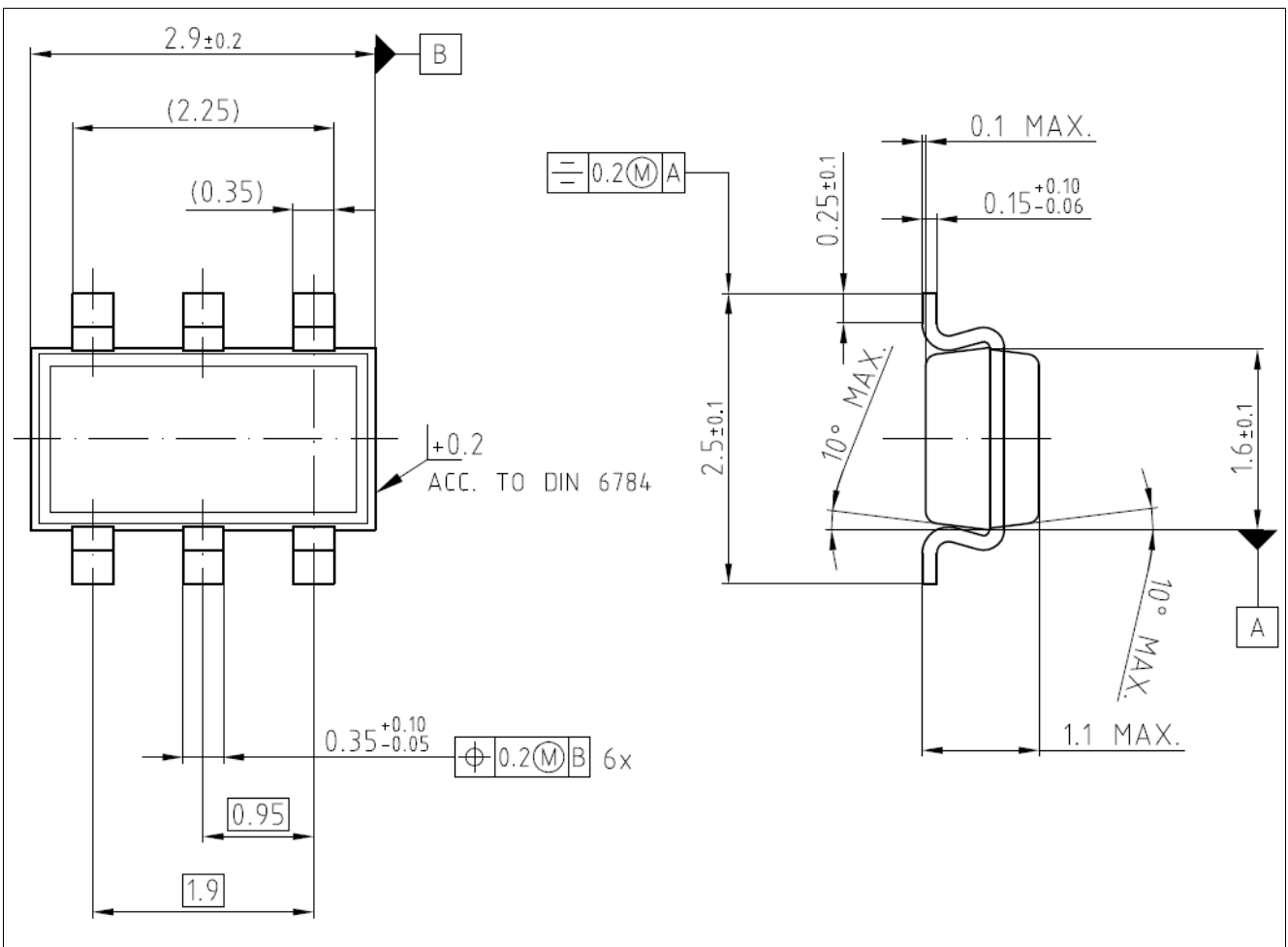


Figure 13 Package Outlines (all dimensions in mm)

Package Information

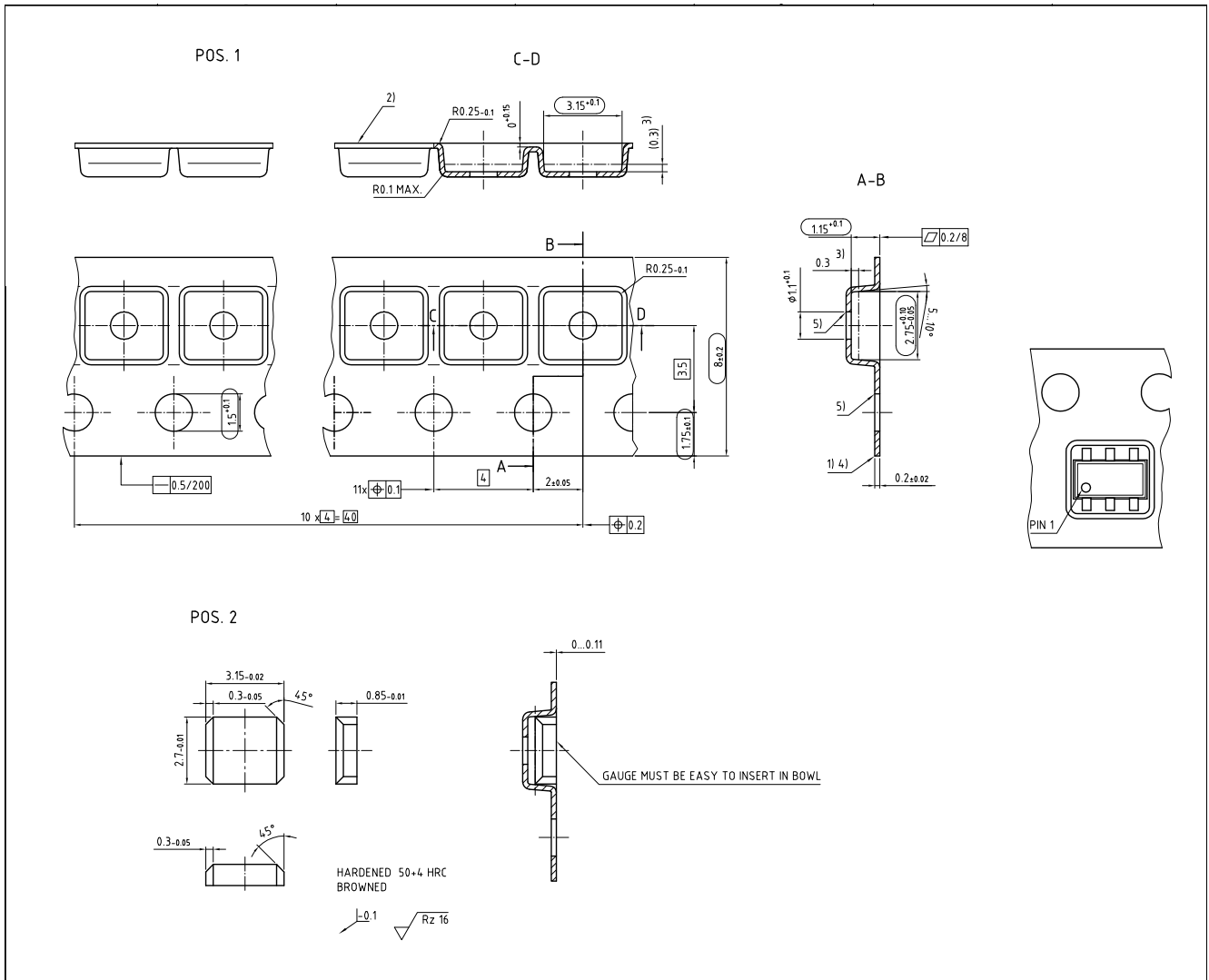


Figure 14 Packing (all dimensions in mm)

Further Information about the package can be found here:

[http://www.infineon.com/cms/packages/SMD\\_-\\_Surface\\_Mounted\\_Devices/TSOP/TSOP6.html](http://www.infineon.com/cms/packages/SMD_-_Surface_Mounted_Devices/TSOP/TSOP6.html)

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Revision History

## 8 Revision History

Revision	Date	Changes
Rev. 1.1	2019-04-09	<b>Table 1</b> updated. <b>Table 5</b> “I <sup>2</sup> C bit clock frequency” deleted, see <b>Table 9</b> . <b>Chapter 3.2</b> rearranged. Missing symbols in electrical-characteristic-tables added. <b>Table 9</b> footnotes added. <b>Table 11</b> footnote <sup>2)</sup> added. <b>Table 12</b> , footnote <sup>2)</sup> editorial changes. <b>Figure 11</b> and <b>Figure 12</b> title updated. Editorial changes.
Rev. 1.0	2016-01-29	Initial version

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